High-Speed DDR4 Memory Designs and Power Integrity Analysis

Cuong Nguyen
Field Application Engineer
cuong@edadirect.com
### PCB Complexity is Accelerating

#### Trends in PCB Complexity

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Min trace/spacing (th)</td>
<td>6.5/6.5</td>
<td>5.4/5.4</td>
<td>4/4</td>
<td>3.9/4.2</td>
</tr>
<tr>
<td>Total metal layers</td>
<td>8</td>
<td>10</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>Total area (in²)</td>
<td>101</td>
<td>76</td>
<td>75</td>
<td>53</td>
</tr>
<tr>
<td># Nets</td>
<td>1465</td>
<td>2952</td>
<td>3411</td>
<td>2109</td>
</tr>
<tr>
<td># Pin-to-pin connections</td>
<td>5190</td>
<td>8813</td>
<td>10960</td>
<td>6228</td>
</tr>
<tr>
<td># Components</td>
<td>649</td>
<td>1981</td>
<td>3400</td>
<td>2608</td>
</tr>
<tr>
<td># Component pins</td>
<td>4214</td>
<td>7760</td>
<td>13505</td>
<td>10122</td>
</tr>
<tr>
<td>Leads / part</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>Leads / in²</td>
<td>42</td>
<td>155</td>
<td>244</td>
<td>304</td>
</tr>
</tbody>
</table>

*Data based on Technology Leadership Awards entry averages*

- Use of Advanced Technologies…
  - HDI (40%), RF/Microwave (26%)
  - Flex/Rigid Flex (9%), Chip-On-Board (11%)
SI/PI Analysis in the Design Flow

**Pre-Layout**
- System Design, Part Selection, Schematic Entry
- Signal Integrity, Crosstalk, EMC, and Timing Analysis

**Layout**
- Full Board Place-and-Route
- Board Partitioning and Critical Net Place-and-route
- Post-layout Signal Integrity, Crosstalk, and EMC Verification

**Prototyping**
- Prototype
- Functional Testing & Debugging
- EMI Testing & Debugging

To eliminate costly $$ design changes here

**Post Layout**
- Design Verification
- Adhering to Constraints
- Finding Design Flaws
- Tuning Pre-emphasis and Equalization

Design Constraints
Technology Investigation
Routing (topology) Options
Stackup Definition

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High-speed PCB Design Issues

• **Signal Integrity**
  - General interfaces
    • Timing, crosstalk, signal quality
  - DDRx
    • Full STA, slew rate derating, write leveling
  - SERDES
    • Loss, impedance discontinuities, BER prediction

• **Power Integrity**
  - DC : do I have enough metal?
    • Voltage drop, high current density, neckdowns
  - AC : do I have enough caps? values?
    • Well-mounted? Good stackup?
    • Impedance profile, noise propagation

• **EMI/EMC**
  - Emission Regulations
Setup/planning – Board Stackup Design

- **Signal Integrity**
  - **Impedance**
    - Highest impedance will drive layer thicknesses
    - Need reference planes for uniform impedance
  - **Loss**
    - Drives trace widths → layer thicknesses
  - **Crosstalk**
    - Drives spacing requirements and routing density

- **Power Integrity**
  - Need enough **thick** planes to minimize DC drop
  - Need **closely-spaced** plane pairs for AC needs
  - Need stitching **vias** to relieve current choke points

- **EMI/EMC**
  - Need **solid** reference planes throughout stackup
Design Considerations

• **Layout/Route**
  – Avoid crossing splits in reference planes (discontinuities)
  – Minimize Inter Symbol Interference (ISI) using matched Impedances
  – Minimize Crosstalk by isolating sensitive bits (ie. Strobes)
  – Match traces within byte lanes (DQ, DM, DQS) to minimize skews

• **Power Supplies**
  – Use precision resistors for \( V_{REF} \)
  – Short/Wide traces to minimize \( L \) and loss
  – 15~25mil clearance from \( V_{REF} \) to adjacent traces to minimize coupling
  – Decouple high frequency Power Supply noise w/caps

• **Signaling**
  – DQ Driver Impedance Matching with proper drive strengths
  – ODT is a must for better Signal Integrity (if not used then use T-branches or dumping resistor to minimize reflections
  – Choose termination carefully to balance power consumption, signal swing, and reflection
  – Use 2T timing for Address/Command
Signal Integrity Analysis

Signal Integrity
Crosstalk
EMC
Eye Diagrams

Sweep Parameters
Impedance/Stackup Planning
Multi-Board
Controller Delays DQ signals internally
DQ & DQS signals are sent “Level” with the Addr/CLK
## Overview – DDR3 vs. DDR4

<table>
<thead>
<tr>
<th></th>
<th>DDR3</th>
<th>DDR4</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VDD/VDDQ/VPP</strong></td>
<td>1.5/1.5/NA (1.35/1.35/NA)</td>
<td>1.2/1.2/2.5</td>
<td>Up to 20% power saving</td>
</tr>
<tr>
<td><strong>Clock Frequencies</strong></td>
<td>400-1600MHz</td>
<td>800-1600MHz+</td>
<td>Higher BW</td>
</tr>
<tr>
<td><strong>CAS Latency</strong></td>
<td>5~14</td>
<td>9~24</td>
<td></td>
</tr>
<tr>
<td><strong>Vref</strong></td>
<td>VDDQ/2 (Ext)</td>
<td>Internal</td>
<td></td>
</tr>
<tr>
<td><strong>DQ Validation</strong></td>
<td>Setup/Hold</td>
<td>Data Eye</td>
<td>Borrowed from SERDES</td>
</tr>
<tr>
<td><strong>Data Termination</strong></td>
<td>VDDQ/2 (VTT)</td>
<td>VDDQ</td>
<td>Asymmetric Term.</td>
</tr>
<tr>
<td><strong>Add/Cmd/Termination</strong></td>
<td>VDDQ/2 (VTT)</td>
<td>VDDQ/2</td>
<td></td>
</tr>
<tr>
<td><strong>I/O Standard</strong></td>
<td>SSTL15</td>
<td>POD12</td>
<td>Power savings on “1” bits</td>
</tr>
<tr>
<td><strong>On Chip Error Detection</strong></td>
<td>No</td>
<td>Parity (Cmd/Add) CRC (DQ)</td>
<td>Server Class</td>
</tr>
<tr>
<td><strong>Bank Grouping</strong></td>
<td>No</td>
<td>4</td>
<td>“Ping-Pong” for efficient use</td>
</tr>
</tbody>
</table>
## Overview – LPDDR3 vs LPDDR4

<table>
<thead>
<tr>
<th></th>
<th>LPDDR3</th>
<th>LPDDR4</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>400-800MHz</td>
<td>800-1600MHz</td>
<td>2x speed (possibly more)</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>12.8GB/s (2ch)</td>
<td>25.6GB/s (2ch)</td>
<td>Higher BW</td>
</tr>
<tr>
<td>VDD2/VDDQ/VDD1</td>
<td>1.2/1.2/1.8</td>
<td>1.1/1.1/1.8</td>
<td>Power reduced 10%</td>
</tr>
<tr>
<td>I/O Interface</td>
<td>HSUL</td>
<td>LVSTL</td>
<td>40% I/O Power reduction vs. POD</td>
</tr>
<tr>
<td>DQ ODT</td>
<td>Vtt Term</td>
<td>VSSQ Term</td>
<td></td>
</tr>
<tr>
<td>CA ODT</td>
<td>No term</td>
<td>VSS Term (optional)</td>
<td></td>
</tr>
<tr>
<td>Vref</td>
<td>External</td>
<td>Internal</td>
<td></td>
</tr>
</tbody>
</table>

- DDR4 to use **Pseudo Open Drain** (POD)
  - Address, Command, Control continue to be SSTL
- LPDDR4 to use **Low Voltage Swing Terminated Logic** (LVSTL)
  - Both Data and Address
### Overview – Speed related Eye challenges

<table>
<thead>
<tr>
<th>Mode</th>
<th>LPDDR1</th>
<th>LPDDR2</th>
<th>LPDDR3</th>
<th>LPDDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>400Mbps</td>
<td>800Mbps</td>
<td>1600Mbps</td>
<td>3200Mbps</td>
</tr>
<tr>
<td>tCK</td>
<td>2.5ns</td>
<td>1.25ns</td>
<td>0.625ns</td>
<td>0.3125ns</td>
</tr>
<tr>
<td>Data eye area</td>
<td>14</td>
<td>1</td>
<td>0.5</td>
<td>0.09</td>
</tr>
<tr>
<td>(Normalized)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Semicon West: High Performance & Low Power Memory Trends – SK Hynix
New Drive Standards – Difference

DDR4

DQ, DQS, DM, TDQS

DDR3

DQ, DQS, DM, TDQS
New Drive Standards – Why?

- Current still flows when driving low

![Diagram showing current flow in DDR4 and DDR3 standards](image-url)
New Drive Standards – Why?

- No current draw when driving a high
Power Savings with DBI

- Ensure more 1’s than 0’s with POD
- If more than 4 bits in a byte are 0, toggle bits
- DBI (Data Bit Inversion) shared with DM => only one feature enabled
- DBI pin is I/O (affects both reads and writes)
PreLayout SI Simulation
**DDRx Routing Guidelines**

- **Constraint-driven routing**
  - Designer knows where the traces should be routed
    - Precise location of traces & vias
    - Control style of routing incl serpentine
e- Things to observe while routing DDRx
  - Width & clearance rules
  - Placement intentions
  - Netline organization
  - Layer restrictions
  - Pad/via entry rules (angle, size)
  - Diff pair rules
Using Sketch routing with DDR3 (video)
Simple Comparison

- Controller -> 50 Ohm T-Line -> DRAM
- Vary DRAM’s ODT to see center level of eye
- 2400Mbps Data rate
DDR3 – sweeping Rx ODT

No change in Center of Eye with ODT
DDR4 – Eye shifting

Eye center shifts with ODT change
Eye center shifts with ODT change
Xilinx VCU108 UltraScale Dev Board
What is Power Integrity?

- **What is a Power Distribution Network (PDN)?**
  - The path (or interconnects) from PWR to ICs (Active Devices)
  - Including PCBs and packages
    - Planes, routed traces, and decoupling capacitors
- **Deliver adequate power from DC->HF**
- **Minimize EMI issues**
- **Provide low-noise reference path for signaling**
Plane Design & the PDN

- Meeting Power Integrity requirements
  - Design PDN (path from power supply to ICs) of low impedance
  - As if an ideal voltage source were directly connected to ICs
  - Use impedance to represent and measure PDN quality
Power Integrity Analysis

- **DC Drop Analysis**
  - Excessive Voltage Drop & High Current Densities
  - Batch Analysis of Supply Nets

- **AC Power Plane Analysis**
  - Capacitor Selection/Mounting
  - Power Supply Impedance

- **Plane Noise Analysis**
  - Voltage Ripples
Power Integrity Optimization (Why?)

- **Reduce Product Costs**
  - Minimizing capacitor BOM (more Caps is worse)
  - Reducing PCB size and layer count
  - Eliminating design iterations
    - Up-front PDN planning & Improve time-to-results

- **Improve Product Reliability**
  - Identifying excessive voltage drop and high current densities at DC
  - Providing stable AC power through capacitor decoupling
DC Drop and Thermal Analysis

• Identify Failures Easily
  – Voltage drop magnitude is easily measured
  – Excessive current density clearly
  – Determine if current density is causing thermal failure

• Create an Optimized Solution
  – How much copper is needed?
  – Optimize component placement?
  – Are additional stitching vias required?
Power Integrity/Thermal Integrity Effects

• Analyze **Joule Heating** effects in traces
  – Identify/localize sensitive area on board
  – Minimize field failures and increase product reliability
Power Integrity Effects
Power Integrity Effects from DDR3 switching

Signal held high

PDN From DDR3 Board

Remaining signals

PRBS @ 2400MT/s

DQS clock @ 1.2GHz
Power Integrity Effects from DDR3 switching

150mV noise from switching of other bits in lane
Integrated Design Flow

- Tight validation for Pre/Post Layout
- Minimize errors, increase accuracy
- Reduce risk and field failures
- Lower cost and reduce time-to-market

SI/PI/Thermal Simulation
Pre/Post

Architectural/Technology Investigation
Performance/Feasibility Analysis
Noise/Crosstalk/Termination/EMI

Constraints

Stackup/Placements
Length/Impedance/via

Board Layout/Route

Constraints

Schematic Design

Library/Symbols
Design Variants

Constraints

• Tight validation for Pre/Post Layout
• Minimize errors, increase accuracy
• Reduce risk and field failures
• Lower cost and reduce time-to-market
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