PCB Fabrication Enabling Solutions
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Military/Aerospace Drove Advanced High Rel Technology...

- C-130
- C-17
- Apache
- JSF
- F-22
- F-18
- MIDS-LVT1
- F-117
- JEM Radio
- KC-135
- T-38
- RAM
- B-2
Until the late 90’s!
Then things really got complicated...

SMV®

DpMV™

DpSMV™

DpBV™

ThermalVia™

FLAT-WRAP™

NextGen-SMV®

HDI-Link™

Sub-Link™
Today’s Agenda

- Market Drivers
  - Array Package Trends
- Enabling PCB Process Technologies
- Advanced Via Structures & Routing Challenges
- NextGen, HDI-Link, & Sub-Link
- Next Generation Microvias
Increasing Complexity

Today’s PCB require a complex blend of many process technologies that must work in concert to provide a solution...

- Small die, shrinking geometries; pushing the limits of annular ring, aspect ratio, and sub 3 mil line & space
- Exponentially increasing I/O; Blind, buried, and laser drilled microvias to increase routing channel density
- Stacking microvias to accommodate fine pitch devices
- Minimizing registration shifts, maximizing resolution
- Optimizing Copper plating (Direct Current vs. Reverse Pulse Plating)
- Materials and lamination limits vs. design constraints
- Improving outer layer etch on multiple lamination designs with FlatWrap
- Thermal management

...The end goal is to put all the pieces together and examine the design and fabrication interactions.
PCB Market Drivers & Array Package Densities
How have Array Packages evolved and what is their impact on PCBs?

Definition of an Array Package:
Array packages are defined as component packages where the I/O’s (Input/Output) or leads can be defined in a “Matrix” pattern in terms of rows and columns. Array packages can provide greatest number of I/O’s per unit area of any package since the entire bottom of the package can be used for connections.

Types of Array Packages
- Pin Grid Arrays “PGA”
- Ball Grid Arrays “BGA”
- Ceramic Column Grid Array “CCGA”
- Land Grid Array “LGA”
- Flip Chip

Design Considerations
- All Array packages present some form of routing challenges in the design process.
- Special consideration must be given to board design with respect to assembly.
Ball Grid Arrays “BGA”

Silicon die encased in molded plastic

Interposer substrate to transform Silicon geometries to PCB geometries. Most often made with PCB process.

Common BGA Pin pitch:

- 1.27 mm
- 0.8 mm
- 0.65 mm
- 0.4 mm
- 1.0 mm
- 0.75 mm
- 0.5 mm
- 0.25 mm

Drilled hole diameter and Pitch are reaching limits and restricting routing.

357 I/O BGA Package

Through hole PCB
Flip Chip (No Package!)

- Flip Chip is the extreme form of an array package. High temperature solder balls are attached directly to the silicon die.
- Extremely fine ball pitch can push the limits of PCB geometries.
- Larger silicon dies cannot tolerate any warpage in the PCB substrate.
- Silicon has a much lower CTE than PCB materials (2.5 PPM vs 18 PPM). To prevent damage to the interconnect on very large silicon die, the PCB must be designed with materials with a lower CTE than conventional epoxy or polyimide materials.

Flip Chip I/O pitch is generally 0.4 mm to 0.2 mm or less.
Density Trends In Array Packages
Assembled Cross-Section Views

**Increasing I/O Density**

1.27 mm BGA package Localized via density 62/cm² (400/in.²)

0.50 mm BGA package Localized via density 400/cm² (2580/in.²)

0.20 mm Flip Chip Localized via density 2500/cm² (16,129/in.²)

20 x 20

6.45 x Increase in via density

6.25 x Increase in via density

Chip Scale Packaging

Flip Chip Packaging
### Circuit Density & Mechanical Drilling limitations

#### Circuit Density vs BGA Pitch (Mechanical Drill)

- **Drill dia.**
  - 1.27 mm: 0.010” (250 µm)
  - 1.0 mm: 0.022” (550 µm)
  - 0.8 mm: 0.008” (200 µm)
  - 0.5 mm: 0.008” (200 µm)

- **Pad dia.**
  - 1.27 mm: 0.010” (250 µm)
  - 1.0 mm: 0.019” (475 µm)
  - 0.8 mm: 0.018” (450 µm)
  - 0.5 mm: 0.018” (450 µm)

- **Line width**
  - 1.27 mm: 0.004” (100 µm)
  - 1.0 mm: 0.004” (100 µm)
  - 0.8 mm: 0.004” (100 µm)
  - 0.5 mm: 0.004” (100 µm)

- **Space**
  - 1.27 mm: 0.004” (100 µm)
  - 1.0 mm: 0.004” (100 µm)
  - 0.8 mm: 0.004” (100 µm)
  - 0.5 mm: 0.004” (100 µm)

- **Thickness**
  - 1.27 mm: Up to 0.100”
  - 1.0 mm: Up to 0.100”
  - 0.8 mm: Up to 0.062”
  - 0.5 mm: Escape Only!

#### Technology Shift

- **Decreasing Channel Density**
  - 1.27 mm
  - 1.0 mm
  - 0.8 mm
  - 0.5 mm

- **Increasing $**
  - 1.27 mm
  - 1.0 mm
  - 0.8 mm
  - 0.5 mm

---

**Notes:**

- **Escape Only!**
Through Hole Routing dilemma for array patterns

Via holes on the perimeter of the pattern form a “Picket Fence” limiting escape if the internal I/O’s.

Perimeter I/O’s have have no escape problem in this case there are 36 perimeter I/O’s.

64 I/O’s require escape

100 I/O BGA Pattern
(Internal vias not shown)
Square Array Escape through Outside Row

Total escape required \( |E_T| = X^2 - 4X + 4 \)

Example: 100 I/O BGA

\[
I/O \text{ via holes per side (Square root of total)}
\]

\[
x \quad 5 \quad 10 \quad 15 \quad 20 \quad 25 \quad 30
\]

\[
y \quad 100 \quad 200 \quad 300 \quad 400 \quad 500 \quad 600
\]
How do we squeeze through the picket fence?

- Determine largest possible via drill diameter with the lowest aspect ratio
- Determine minimum pad diameter to achieve IPC Class II, tangency, or IPC Class III
- Maintain a minimum of 8 mils from the primary drill hole edge to any copper features
- Signal routing channels come in integer values (i.e. 1,2,3,...n)
  - Track width and pad diameter should be maximized to take advantage of via or device pitch with respect to the maximum integer value of signal routes (in other words, don’t shrink pads and or track widths if it does not create another signal route !)
  - Signal track width should be selected based on the electrical requirements
Array Pattern Escape, Through-hole IPC Class 2

1.27 mm: 3 Track
- 10 mil drill
- 20 mil pad
- 4 mil track

1.0 mm: 2 Track
- 10 mil drill
- 20 mil pad
- 4 mil track

0.8 mm: 1 Track
- 8 mil drill
- 18 mil pad
- 3.5 mil track

0.5 mm: 0 Track
- 6 mil drill
- 14 mil pad
- No routing
# Annular Ring Requirements For IPC Class 2 & 3

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Class 2</th>
<th>Class 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>External</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Plated-through holes</td>
<td>Not greater than 90° breakout of hole from land when visually assessed.¹</td>
<td>The minimum annular ring <strong>shall</strong> be 50 μm [1,969 μin].</td>
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<td></td>
<td>The land/conductor junction <strong>shall not</strong> be reduced below the allowable width reduction in 3.5.3.1.</td>
</tr>
<tr>
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<td></td>
<td>The minimum external annular ring <strong>shall</strong> be 25 μm [984 μin].</td>
</tr>
<tr>
<td><strong>Internal</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Plated-through holes</td>
<td>90° hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.¹</td>
<td>The minimum internal annular ring <strong>shall</strong> be 25 μm [984 μin].</td>
</tr>
<tr>
<td><strong>External</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unsupported holes</td>
<td>Not greater than 90° breakout of hole from land when visually assessed.¹</td>
<td>The minimum annular ring <strong>shall</strong> be 150 μm [5,906 μin].</td>
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<td></td>
<td>The minimum external annular ring may have a 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes, or splay in the annular ring of isolated areas.</td>
</tr>
</tbody>
</table>

Annular Ring requirement drives pad diameter
Drill diameter +10 Mils (up to 100 mils thick) = pad diameter IPC Class 2
Pad diameter +10 Mils = anti-pad diameter
Annular Ring Measurement

External annular ring is measured from the inside of the plated through hole barrel to the edge of the land pad.

Non-Teardrop pad

Internal annular ring is measured from the hole barrel to the edge of the land pad.

Teardrop pad to maintain required minimum trace connection when breakout is allowed.

IPC 6012C Breakout definition:

\[ A = 1.414 \times \text{Radius of PTH} \]
\[ B = \text{Diameter of PTH} \]
Annular Ring Requirements For IPC Classes II & III

IPC 6012C  Class 2

- Minimum annular Ring 1.969 mil
- 90 degree Breakout

IPC 6012C  Class 3

- Larger pad than Class II to allow For registration
- Minimum annular Ring 0.984 mil

Worst case registration allowed by IPC Class II

Worst case registration allowed by IPC Class III
Minimum Drilled Hole To Copper & Minimum Class II Pad

- 10 mil drill 20 mil pad
- 10 mil drill 20 mil pad
- 10 mil drill 20 mil pad
- 10 mil drill 20 mil pad
- 10 mil drill 20 mil pad
- 10 mil drill 20 mil pad
- 10 mil drill 20 mil pad
- 10 mil drill 20 mil pad
- 10 mil drill 20 mil pad

- Internal pad designed for tangency
- Drilled hole to copper of 8 mils
- 3 mil space maintained

- Internal pad designed minimum with breakout
- Drilled hole to copper of 7 mils
- 3 mil space can be violated
Array Pattern Routing for BGAs

0.65 mm BGA

Through-hole Vias

0.016” (400 µm) via pad
0.008” (200 µm) drill
0.003” (75 µm) trace
0.0033” (83 µm) space

0.0073” (185 µm) drill-to-copper
Violates hole-to-copper min
Break-out allowed
Requires additional Engineering $$$$$$

Thickness of 0.028” (0.711 mm) - 0.062” (1.575 mm)

Internal Layer

Aspect Ratio 7.75:1

TTM Technologies
Mechanical Drilling: How small can we go?

- Alignment issues
- Drill wander
- Drill life
- Hole quality

Same process, smaller drills!
Putting Small Diameter Drills Into Perspective

- Human hair: 2.5 mil (60 micron) to 3.5 mil (90 micron)
- Carbide drill bit: 5.9 mil (150 micron)

- Small diameters are very fragile
- High speed spindles are required
- Feed rates are about 50% of standard via diameters
- Drill life of 300 to 600 hits depending on material
- Short flute length limits hole depth
- Drill cost is higher
- Limited availability from offshore PCB production
Array Pattern Escape: Through Hole IPC Class 2

1.27 mm: 3 Track
10 mil drill
20 mil pad
4 mil track

1.0 mm: 2 Track
10 mil drill
19.4 mil pad
4 mil track

0.8 mm: 1 Track
8 mil drill
18 mil pad
4.5 mil track

0.5 mm: 0 Track
6 mil drill
16 mil pad
No routing

What now?
Enabling PCB Equipment

- Laser Drilling
- Laser Direct Imaging
- Reverse Pulse Plating
Laser Drilling Technology Overview

- Hole diameters range from 4 to 8 mils and are typically in the 5 to 6 mil range.
- Pad sizes are reduced (via +5 or 6 mil, instead of +10 mil), leaving more space for routing and smaller antipads.
- Hole depth is limited by copper plating aspect ratio, typically 0.5: to 0.6:1 however higher aspect ratios can been achieved.
- Both YAG and CO₂ lasers are used for PCB drilling. YAG lasers are in the ultra violet spectrum and can drill both copper and dielectric. CO₂ lasers are in the infrared spectrum and can drill dielectric materials.
- The combined use of YAG and CO₂ lasers allow lasing of all common PCB materials at optimum speed.
- Three step lasing operation provide optimum hole quality i.e. YAG to remove copper, CO₂ to remove dielectric and YAG to clean the copper pad.
- It is not practical to laser drill all the way through a board unless it is less than about 10 mils thick.
Laser Drilling Technology: The Quest For Speed!

**Combination ND:YAG CO₂**
Forms holes by removing copper with the ND:YAG laser and the dielectric and re-enforcing material with the CO₂ laser (Approximately 3,500 to 13,000 holes per minute)

**CO₂ (Infrared)**
Capable of drilling most re-enforcing materials and laminate resin systems. Not effective for drilling copper (copper is reflective in the infrared spectrum and must be window etched) Forms holes by pulsing a larger high energy beam (Approximately 17,000 holes per minute)

**ND:YAG (Ultra-Violet)**
Capable of drilling copper, all re-enforcing materials and all laminate resin systems. 25 to 50 micron beam forms holes by spiraling, or trepanning, the beam (Approximately 600 to 1,400 holes per minute)
Laser Drilled Hole Geometry

Typical Via Diameter

Termination or “Capture Pad”

Laser drilled Microvia
Layer 1 to 2

0.005”
0.006”

Maximum Via Diameter

Laser drilled Microvia
Layer 1 to 3

0.008”

Note:
1- Hole depth is limited by plating aspect ratio (depth/diameter)
   Typical aspect ratio on laser drilled holes is 0.5:1 to 0.6:1 max
2- Holes greater than 0.005” are generally considered too large
to be placed in component pad
Array Pattern Routing: Microvia

1.0 mm: 3 Track
- 5 mil Laser
- 10 mil pad
- 4 mil track

0.8 mm: 2 Track
- 5 mil Laser
- 10 mil pad
- 4 mil track

0.5 mm: 1 Track
- 5 mil Laser
- 10 mil pad
- 3 mil track

0.4 mm: 0 Track
- 5 mil Laser
- 10 mil pad
- No track

Routing is possible with smaller internal pads and sub 3 mil lines reducing yields

What now?
Routing By Via Row Reduction

Once routing channels are eliminated by current process limitations, each row of the array pattern will require a unique routing layer. As each row is connected it will open routing for the next.

This approach dramatically increases PCB complexity!
Second Generation Microvia Geometries: Routing by via row reduction

Example of 100 I/O 0.4 mm Pitch Fan out Inverted Pyramid Approach
Stacked MicroVias
Layer 1 - 2
Layer 2 - 3
Layer 3 – 4
Layer 4 – 5
Layer 5 – 6
0.011” pad internal
0.005” laser drill
Solid copper plate

Stacked MicroVias
Layer 13 – 12
Layer 12 – 11
Layer 11 – 10
Layer 10 – 9
Layer 9 - 8
0.011” pad internal
0.005” laser drill
Solid copper plate

Finish Thickness = 0.054” +/- 0.005”
Material = Isola 370 HR

0.4 mm BGA Advanced Construction 5 lams

Layer 5-8 = through holes
0.016” pad
0.006” drill

Layer 1-12 = through holes
0.018” pad
0.008” drill

Solder mask
Layer 1 Mixed
Layer 2 Mixed
Layer 3 Plane
Layer 4 Sig
Layer 5 Sig
Layer 6 Plane
Layer 7 Plane
Layer 8 Sig
Layer 9 Sig
Layer 10 Plane
Layer 11 Mixed
Layer 12 Mixed
Solder mask

Solid copper plate

0.0028” Ref.

0.005” Ref.

0.4 mm BGA Advanced Construction 5 lams

TTM Technologies
Stacked MicroVia (SMV®)

0.4 mm BGA Advanced Construction

Finish Thickness = 0.0315" +/- 0.004" (0.8 mm)
Material = Isola 370 HR
Stacked MicroVias
Layer 1 - 2
Layer 2 – 3
Layer 3 – 4
Layer 10 - 9
Layer 9 – 8
Layer 8 - 7
225 µm (0.009”) pad external
200 µm (0.008”) pad internal
88 µm (0.0035”) trace & space external
65 µm (0.00255”) trace & space internal

Finish Thickness = To be Defined
Material = 370 HR

Layer 4 – 7 buried via
0.008” drill
0.018” pad

3/8 oz copper plates to 15 µm - 20 µm (0.0006” - 0.0008”)
Current HDI designs require adaptive tooling to meet registration and resolution requirements.

Laser Direct Imaging (LDI) relies on soft tooling eliminating the need for photo tools (Film) saving time and recycling costs of silver base films.

LDI is an off contact imaging method allowing extremely high resolution.

Since LDI is a “soft tooling process” every image can individually registered and scaled for material compensation.

Increased accuracy allows smaller pad diameters while achieving annular ring requirements.

Precision solder mask registration can be achieved with LDI.
The minimum photo tool opening is limited by the ability to image and fully remove unexposed resist in the narrow gap between traces with high yield.
Laser Direct Imaging (LDI)

- Elimination of Photo Tools
- No Film/Artwork Movement
- Quick Turn Made Easy
  - Run product as soon as Engineering releases data to the floor
- Reduction in Defect Count
  - Direct Write = No Film related defects
  - No issues related to loss of vacuum

- Improved Resolution, 4000 dpi
- Current process capability (<0.0025”/0.0025”)
- CCD Camera System & Target Fiducials
  - Improved Registration
- Positional Accuracy +/-25µm (.001in)
Laser Direct Imaging (LDI)

Precise Inner Layer Registration

24 Layer PCB Cross-Section
Laser Direct Imaging (LDI) Solder Mask (Optional Process)

- Laser Direct Imaged Solder Mask
  - Adaptively tooled
  - Improved Registration +/- 0.001” vs. +/- 0.003”

Consult TTM Engineering For Detailed Information Prior to Design
Advanced Plating Capabilities For HDI

- HDI Circuits often require a variety of different plating operations to meet design requirements
- High quality copper plating is essential for via reliability
- High aspect ratio plated through-holes, microvias, controlled depth holes and solid copper vias present many challenges for electroplating
- Some via structures can require several plating cycles increasing production time and product cost
- Reverse Pulse Plating is the building block to address these challenges
Example 1. Mechanically drilled through hole that will be used to penetrate the entire thickness of the PCB or a through hole that will be used in a mechanically drilled sub-lamination used to form blind or buried via’s. In this configuration the depth of the hole is measured from the surface of the external copper layers. In this case if the hole diameter was 0.010” and the depth was 0.093” the Aspect Ratio would be 9.3 to 1
Aspect Ratio: Microvia & Controlled Depth Drilling

Example 2. Laser drilled microvia’s are a controlled depth hole that terminates on a copper layer. As a result the depth of the hole is calculated from the top of the terminating layer to the top of the copper foil layer on the hole entrance. In this case if the hole diameter was 0.006” and the depth was 0.003” the Aspect Ratio would be 0.5 to 1.

Example 3. Controlled depth mechanically drilled hole that terminates to an internal copper layer. In this case the mechanically drilled hole must penetrate the internal copper layer in order to make a reliable connection. In order to insure the internal layer penetration, the dielectric thickness and drill depth tolerance must be taken into account and the worst case depth must be used in the calculation. In this case if the hole diameter was 0.025” and the depth was 0.010” the Aspect Ratio would be 0.4 to 1.
Limitations With Conventional “DC” Copper Electroplating

- In conventional DC electroplating, edges of the hole barrel have easy access for copper ions to deposit resulting in higher current density and faster copper deposition.

- Regions deep in the hole barrel have a lower current density resulting in a lower deposition rate. The net result on high aspect ratio holes is that copper tends to be thicker at the edge of the hole barrel for a given thickness at the center.

- Reducing the overall current density can achieve more uniform plating thickness. However, if the current density is reduced too much the grain structure of the copper can become coarse leading to possible barrel cracking.
Increasing layer counts and reduced hole diameters are driving Aspect Ratios beyond limits of standard electroplating. Solution: Complex Waveform Pulse Plating. Copper deposition is enhanced by modifying the plating chemistry in the reverse current cycle to reduce copper deposition in high current density areas of the hole barrel, resulting in uniform plating.
High Aspect Ratio Reverse Pulse Plating Process

Simplified Overview:

In the forward cycle Cu deposition is greater in high current density areas and lower in the center of the hole barrel. In the reverse cycle the brighteners are de-sorbed from the high current density areas slowing Cu deposition and then slowly return to the surface. This process continues resulting in fast uniform copper deposition.
High Aspect Ratio Copper Electroplating  Reverse Pulse Plating Process

Reverse pulse plating provides uniform copper plating in both high aspect ratio through holes as well as blind laser drilled and mechanical formed blind holes.

Aspect Ratio = 14:1
Thickness = 0.112”
Drill dia. = 0.008”

Aspect Ratio = 16:1
Thickness = 0.216”
Drill dia. = 0.0135”

Controlled depth mechanical drilling

0.005” Laser drilled microvia
High Aspect Ratio Copper Electroplating Reverse Pulse Plating Process

### Reverse Pulse Plating Capabilities

<table>
<thead>
<tr>
<th>Description</th>
<th>Aspect ratio</th>
<th>Via/Hole Diameter</th>
<th>Dielectric/Board Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microvia</td>
<td>0.6:1</td>
<td>100 µm (0.004”)</td>
<td>100 µm (0.004”)</td>
</tr>
<tr>
<td>PTH</td>
<td>11:1</td>
<td>200 µm (0.008”)</td>
<td>2.8 mm (0.112”)</td>
</tr>
<tr>
<td>PTH</td>
<td>14:1</td>
<td>&gt;337.5 µm (&gt;0.0135”)</td>
<td>5.4 mm (0.216”)</td>
</tr>
</tbody>
</table>

#### Notes:

1. Always consult engineering with any application where the emerging capabilities are required
2. Requires special process and may not work on all applications
3. Extended flute length drills required, Typical dielectric thickness limit 1.57 mm (0.062”)

Reverse Pulse Plating Line
Achieving Higher Densities Using Advanced Via Structures
Once you leave through-hole designs, the goal is to find the via combination that maximizes routing channel density at the lowest cost.

**Mechanical Solution**
- Controlled Depth Drill: Still geometry limited, Limited Z axis connectivity
- Blind & Buried vias: Channel density enhanced, Still geometry limited, Limited Z axis connectivity

**Laser Solution**
- Microvias: Channel density enhanced through smaller geometry, Limited Z axis connectivity
- Stacked Microvia: Channel density enhanced through smaller geometry, Unlimited Z axis connectivity

Standard through hole technology: Channel density limited by via density, geometry and pitch.
• Increased channel density on layers below the controlled depth drill
• Standard PTH geometry apply, Depth limited by aspect ratio
• No sequential lamination required
Via Structures: Laser Modified Controlled Depth Drill

- Increased channel density on layers below the controlled depth drill
- Allows a connection with no stub
- Standard PTH geometry apply, Depth limited by aspect ratio
- No sequential lamination required

Via hole is first mechanically drilled then with a laser the remaining dielectric is removed clearing a path to the copper layer.
Via Structures: Blind Via

- Increased channel density on lower sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles
- Increased channel density on sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles
- No Z axis connectivity between adjacent sub-laminations
Increased channel density on layer 1 and 2 from reduced geometry
Increased channel density on layers n-1 to n resulting from a blind hole
Standard PTH geometry apply to mechanical drilled holes
Dielectric thickness layer 1:2 limited by plating aspect ratio (0.5:1 to 0.6:1)
First Generation Microvia Geometries: (Microvia terminating on a foil layer)

<table>
<thead>
<tr>
<th>Microvia Feature Variables</th>
<th>Copper Foil Weight</th>
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<tbody>
<tr>
<td></td>
<td>1/4 oz</td>
</tr>
<tr>
<td></td>
<td>3/8 oz</td>
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<tr>
<td></td>
<td>1/2 oz</td>
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<tr>
<td></td>
<td>1.0 oz</td>
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<tr>
<td>Layer 1 Copper Foil W1 ²</td>
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<tr>
<td>Minimum Pad Diameter ¹</td>
<td>D1</td>
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<tr>
<td>Pad Thickness: W1 + T1</td>
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<tr>
<td></td>
<td>0.008&quot;</td>
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<td>0.008&quot;</td>
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<td>0.0024&quot;</td>
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<tr>
<td>Layer 2 Copper Foil W2 ²</td>
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<td>Minimum Space to Trace ⁴</td>
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<td>Minimum Capture Pad Dia. ¹, ⁵</td>
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<td>Minimum Laser Drill Diameter ³</td>
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<td>Dielectric Thickness</td>
<td>H1</td>
</tr>
<tr>
<td></td>
<td>0.004&quot;</td>
</tr>
<tr>
<td></td>
<td>0.006&quot;</td>
</tr>
<tr>
<td></td>
<td>0.0025&quot;</td>
</tr>
<tr>
<td></td>
<td>0.003&quot;</td>
</tr>
<tr>
<td>Cu Plating Thickness</td>
<td>T1</td>
</tr>
<tr>
<td></td>
<td>0.0012&quot;</td>
</tr>
</tbody>
</table>

Notes:
1- Recommended minimum pad diameters are drill diameter + 0.006”
2- 3/8 oz and 1/2 oz Cu foil weight are recommended (design permitting)
3- Larger hole diameter can be achieved with an increase in lasing and plating time
4- Minimum pad to trace assumes that the trace will pass the pad tangentially
5- 3/8 oz copper foil is not recommended for laser capture pad layers (non-Plated)
First Generation Microvia Geometries: (Microvia terminating on a foil layer)

Lowest cost due to one lamination cycle

Finish Thickness = 0.062 +/- 0.006
Material = High Temp FR4

Layer 1 – 8 through vias
0.020” pad & 0.010” drill
Increased channel density on layer 1 and 2 from reduced geometry

Increased channel density on layers n-1 to n resulting from a blind hole

Standard PTH geometry apply to mechanical drilled holes

Dielectric thickness layer 1:2 limited by plating aspect ratio (0.5:1 to 0.6:1)
# First Generation Microvia Geometries:
(Microvia terminating on a plated layer)

## Microvia Feature Variables

<table>
<thead>
<tr>
<th>layer 1 Copper Foil W1</th>
<th>D1</th>
<th>Minimum Pad Diameter</th>
<th>Pad Thickness: W1 + T1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/4 oz</td>
<td>0.008&quot;</td>
<td>0.0014&quot;</td>
<td>0.008&quot;</td>
</tr>
<tr>
<td>3/8 oz</td>
<td>0.008&quot;</td>
<td>0.016&quot;</td>
<td>0.010&quot;</td>
</tr>
<tr>
<td>1/2 oz</td>
<td>0.010&quot;</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>1.0 oz</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>layer 2 Copper Foil W2</th>
<th>D2</th>
<th>Minimum Space to Plane</th>
<th>Minimum Capture Pad Dia.</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>0.005&quot;</td>
<td>0.008&quot;</td>
<td>0.008&quot;</td>
</tr>
<tr>
<td>S2</td>
<td>0.003&quot;</td>
<td>0.003&quot;</td>
<td>0.0035&quot;</td>
</tr>
<tr>
<td>D3</td>
<td>0.008&quot;</td>
<td>0.008&quot;</td>
<td>0.010&quot;</td>
</tr>
<tr>
<td></td>
<td>0.0013&quot;</td>
<td>0.0014&quot;</td>
<td>0.0016&quot;</td>
</tr>
</tbody>
</table>

## Copper Foil Weight

<table>
<thead>
<tr>
<th>Layer 1 Copper Foil W1</th>
<th>Layer 2 Copper Foil W2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/4 oz</td>
<td>3/8 oz</td>
</tr>
<tr>
<td>1.0 oz</td>
<td>1.0 oz</td>
</tr>
</tbody>
</table>

## Notes:

1- Recommended minimum pad diameters are drill diameter + 0.006”
2- 3/8 oz and 1/2 oz Cu foil weight are recommended design permitting
3- Larger hole diameter can be achieved with an increase in lasing and plating time
4- Non-standard increased plating thickness (Wrap plating etc..) will increase minimum space
5- Minimum pad to trace assumes that the trace will pass the pad tangentially
First Generation Microvia Geometries: ("Staircase" Structure)

Layer 1 - 2 = Offset Microvias
0.012” pad & 0.006” laser drill

Layer 2 - 7 = Buried Vias
0.018” pad & .008” drill

Layer 1 - 8 = Through-hole
0.020” pad & .010” drill

Material = High temp FR4

Finish Thickness = 0.062” +/- 0.006”
Example: Two layer offset “Staircase” microvia structure making a connection from layer 1 to Layer 3. Microvias from layer 2 to 3 does not require a plated copper fill, whereas the microvia from layer 1 to 2, copper fill is optional but recommended for via-in-pad. H1 and H2 represent the dielectric thickness between layers and standard design rules apply.

1- Layer two consists of the 1:2 capture pad and the 2:3 land pad positioned tangent to each other. In order to avoid an acute angle between the two round geometries a fillet is required to make an oblong pad.
Finish Thickness = 0.062” +/- 0.006”
Material = High temp FR4
First Generation Microvia Examples:
Microvia Through Hole Combo 1.0 mm
First Generation Microvia Examples:
microvia & Buried & PTH Vias 1.0 mm (Min Offset)

- **Ball pad**
- **Laser drilled hole**
- **Buried via (2:N-1)**

One track Route Between Capture pad and buried via

- **30 mil anti-pad**
- **12 mil capture pad**

10 mil drill, 20 mil pad
First Generation Microvia Examples: Microvia Through Hole Combo 0.8 mm

- Two track routing
  - Layer 2
- Ball pad
- High density
  - Routing layer
- One track routing
  - Layer 1
- 0.8 mm
- 10 mil drill
- 20 mil pad
- 1 mm pitch
- 3 mil max.
- No limit!
- 65
First Generation Microvia Examples:
Microvia Through Hole & Buried Combo 0.8 mm

- Buried via 8 mil drill 18 mil pad
- Ball pad
- One track between PTH’s
- One track routing Layer 2 on 45 degree
- 3 mil max.
- No limit!
- 10 mil drill 20 mil pad 1 mm pitch
- 0.8 mm
First Generation Microvia Examples:
Microvia Through Hole & Buried Combo 0.8 mm

- **Buried via**
  - 8 mil drill
  - 18 mil pad

- **Ball pad**
  - No Via

- **One track between PTH’s**

- **Plane Connection**
  - 10 mil drill
  - 20 mil pad
  - 1 mm pitch

- **One track routing**
  - 3 mil max.
  - No limit!
First Generation Microvia Examples:
Microvia “Stair Case” & Buried Combo 0.8 mm

Buried via
10 mil drill
20 mil pad

One track between PTH’s

Ball pad
10 mil drill
20 mil pad
1 mm pitch

One track routing Between “Stair Case”

3 mil max.
3 mil max.

0.8 mm
First Generation Microvia Examples:
Microvia “Stair Case” & Buried Combo 0.8 mm

- Buried via
  - 10 mil drill
  - 20 mil pad

- Plane Connection
  - 10 mil drill
  - 20 mil pad
  - 1 mm pitch

- “Stair-Case” Connection through a plane layer

- Plane Layer two

- One track between PTH’s

- 3 mil max.

- 3 mil max.
Limitation of first generation microvias

Solder Joint Quality & Reliability...Via-In-Pad Micro Via

Ideal Solder Joint

- Microvias vias in pad from layer 1 to 2 must have minimum volume after plating to prevent and or minimize solder voiding due to trapped volatiles
- Even with minimum microvia volume an optimized solder profile is often necessary
- Microvia in excess of 0.005” are too large for via in pad and generally result in solder voiding
Mechanical Via-In-Pad & Microvia Routing Geometries

Mechanical via-in-pad requires wrap plating to meet the requirements of IPC 6012. This increases minimum line width and spacing that can be achieved due to increased copper thickness, in general greater than 5 mil line and space. Microvia Designs generally require line width and space less than 5 mils. There is a conflict?

Mixed Signal Design

- Chip Scale Digital
  - Microvia
  - Stacked microvia
  - 3 mil line and space

- Analog RF/Microwave
  - Via-In-Pad
  - Critical line & Space
  - Via stub removal
  - Mixed depth blind via
  - Multiple wrap plating

Design Conflict!
Second Generation
Microvias & Applications
First and Second Generation Laser Drilled Microvia Structures

2-4-2 HDI Substrate

1:3 uVia → 1:2 uVia → 1:3 Stacked plate fill uVia

2 Layer HDI buildup

4 Layer MLB core

1:2 2:3 Staircase uVia

First Generation Microvia Structures ↔ Second Generation Microvia Structures
Polymer Filled Microvias
Not Recommended due to Reliability Concerns

Basic process for polymer fill
- Laser drill
- Electroless copper
- Electroplate copper
- Polymer fill
- Planarize
- Electroless copper
- Pattern plate

Advantages
- Less capital equipment
- No special chemistry

Disadvantages
- Very difficult to get high percentage fill
- Wrap plating is required
- Many process steps

Stacked Microvia using polymer fill and copper over-plate
Recommended Fill Method: Solid Copper

Mechanism of copper filling

- Bottom-up filling behavior is attributed to the action of organic additives (must be controlled to prescribed limits)

- Suppressor rapidly forms current inhibiting film on Cu surface. Film has little geometric dependence due to high suppressor solution concentration

- Accelerated bottom-up fill behavior is due to a local accumulation of brightener species at the feature base

- As surface area is reduced during deposition, the concentration of brightener species increases, resulting in a non-equilibrium surface concentration. This local concentration of brightener accelerates the plating rate relative to the surface.

Source: Mechanism of copper filling

Planar Microvia

Stacked Microvia

Brightener
Carrier
Advanced process plating room for solid copper via fill
Advanced PCB Structures using Stacked Microvias

- Solid copper microvias can be vertically stacked to gain deeper penetration to internal layers (Design Flexibility)

- In general, laser direct imaging is recommended for proper registration in high density PCB applications

- Stacked microvias require sequential lamination for each additional layer

- The number of vertically stacked layers is limited by the number of lamination cycles that materials are exposed to. In general, most laminates should not be exposed to more than three thermal lamination cycles (4 – 5 Advanced)

- Stacked microvias start with a plating cycle to develop a solid copper filled via, followed by a pattern plate cycle to produce the circuit image. Therefore, the pattern plate thickness must be accounted for in the circuit design
# Second Generation Microvia Geometries:

**Solid Via Landing on a Non-Plated Layer – Design Guidelines**

---

**Microvia Feature Variables**

<table>
<thead>
<tr>
<th>Layer 1 Copper Foil W1</th>
<th>1/4 oz</th>
<th>3/8 oz</th>
<th>1/2 oz</th>
<th>1.0 oz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Pad Diameter</td>
<td>D1</td>
<td>0.008&quot;</td>
<td>0.008&quot;</td>
<td>0.010&quot;</td>
</tr>
<tr>
<td>Pad Thickness: W1 + T1</td>
<td></td>
<td>0.0014&quot;</td>
<td>0.0016&quot;</td>
<td>0.0018&quot;</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Layer 2 Copper Foil W2</th>
<th>1/4 oz</th>
<th>3/8 oz</th>
<th>1/2 oz</th>
<th>1.0 oz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Space to Plane</td>
<td>S1</td>
<td>N/A</td>
<td>0.0035&quot;</td>
<td>0.004&quot;</td>
</tr>
<tr>
<td>Minimum Space to Trace</td>
<td>S2</td>
<td>N/A</td>
<td>0.003&quot;</td>
<td>0.0035&quot;</td>
</tr>
<tr>
<td>Minimum Capture Pad Dia.</td>
<td>D3</td>
<td>N/A</td>
<td>0.008&quot;</td>
<td>0.010&quot;</td>
</tr>
<tr>
<td>Foil Thickness</td>
<td>W2</td>
<td>N/A</td>
<td>0.00045&quot;</td>
<td>0.0006&quot;</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Laser Drill Diameter</td>
<td>D2</td>
</tr>
<tr>
<td>Dielectric Thickness</td>
<td>H1</td>
</tr>
<tr>
<td>Cu Plating Thickness</td>
<td>T1</td>
</tr>
</tbody>
</table>

---

**Notes:**

1. Recommended minimum pad diameters are drill diameter + 0.006”
2. 3/8 oz and 1/2 oz Cu foil weight are recommended (design permitting)
3. Larger hole diameter can be achieved with a significant increase in lasing and plating time
4. Minimum pad to trace assumes that the trace will pass the pad tangentially
Second Generation Microvia Geometries:

Solid Via Landing on a Non-Plated Layer

Finish Thickness = 0.062” +/- 0.006”
Material = High Temp FR4
## Second Generation Microvia Geometries:

### Solid Via Landing on a Plated Layer – Design Guidelines

**Features and Variables:**
- **Microvia Feature Variables**
- **Copper Foil Weight**
- **Minimum Pad Diameter**
- **Pad Thickness: W1 + T1**
- **Minimum Space to Trace**
- **Minimum Capture Pad Diameter**
- **Plated Layer Thickness: W2 + T2**

### Table:

<table>
<thead>
<tr>
<th>Microvia Feature Variables</th>
<th>1/4 oz</th>
<th>3/8 oz</th>
<th>1/2 oz</th>
<th>1.0 oz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 1 Copper Foil W1</td>
<td>D1</td>
<td>0.008&quot;</td>
<td>0.008&quot;</td>
<td>0.010&quot;</td>
</tr>
<tr>
<td>Minimum Pad Diameter</td>
<td></td>
<td>0.0014&quot;</td>
<td>0.0016&quot;</td>
<td>0.0018&quot;</td>
</tr>
<tr>
<td>Pad Thickness: W1 + T1</td>
<td></td>
<td>0.0014&quot;</td>
<td>0.0016&quot;</td>
<td>0.0018&quot;</td>
</tr>
<tr>
<td>Layer 2 Copper Foil W2</td>
<td>S1</td>
<td>0.005&quot;</td>
<td>0.005&quot;</td>
<td>0.006&quot;</td>
</tr>
<tr>
<td>Minimum Space to Trace</td>
<td></td>
<td>0.003&quot;</td>
<td>0.003&quot;</td>
<td>0.0035&quot;</td>
</tr>
<tr>
<td>Minimum Capture Pad Dia.</td>
<td></td>
<td>0.008&quot;</td>
<td>0.008&quot;</td>
<td>0.010&quot;</td>
</tr>
<tr>
<td>Plated Layer Thickness</td>
<td>D3</td>
<td>0.0013&quot;</td>
<td>0.0014</td>
<td>0.0016</td>
</tr>
<tr>
<td>Minimum Space to Plane</td>
<td></td>
<td>0.0013&quot;</td>
<td>0.0014</td>
<td>0.0016</td>
</tr>
<tr>
<td>Maximum Space to Trace</td>
<td></td>
<td>0.0022&quot;</td>
<td>0.0016</td>
<td>0.0022</td>
</tr>
<tr>
<td>Laser Drill Diameter</td>
<td>D2</td>
<td>0.004&quot;</td>
<td>0.006&quot;</td>
<td></td>
</tr>
<tr>
<td>Dielectric Thickness</td>
<td>H1</td>
<td>0.0025&quot;</td>
<td>0.003&quot;</td>
<td></td>
</tr>
<tr>
<td>Cu Plating Thickness</td>
<td>T1</td>
<td>0.0012&quot;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Copper Plating Thickness</td>
<td>T2</td>
<td>0.001&quot;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Notes:
1. Recommended minimum pad diameters are calculated as drill diameter + 0.006”
2. 3/8 oz and 1/2 oz Cu foil weight are recommended design permitting.
3. Larger hole diameter can be achieved with a significant increase in lasing and plating time.
4. Non-standard increased plating thickness (Wrap plating etc.) will increase minimum space.
5. Minimum pad to trace assumes that the trace will pass the pad tangentially.
Second Generation Microvia Geometries:
Solid Via Landing on a Plated Layer

Layer 1 - 2 & 8-7 - Microvias
0.012” pad & 0.006” laser drill

Layer 2 - 7 = Buried Vias
0.018” pad & 0.008” drill

Layer 1 - 8 = Through-hole
0.020” pad & 0.010” drill

Finish Thickness = 0.042” +/- 0.004”
Second Generation Microvia Geometries: Stacked Microvia Examples

Example 1: Two layer stacked microvia (+2) terminating on a copper foil shown with a copper plate-fill on the layer 1 to layer 2 via for via-in-pad application. H1 and H2 represent the dielectric thickness between layers and standard design rules apply.

Example 2: Two layer stacked microvia (+2) terminating on a plated layer. This example illustrates how the internal solid copper vias become the building block for the vias on top until you get to the layer 1 to 2 via. The final 1 to 2 via has the option to be filled with copper (recommended for via-in-pad) or they can be left as a standard via with a divot if used as an interstitial via. H1 and H2 represent the dielectric thickness between the layers where standard microvia rules apply.
Second Generation Microvia Geometries:

Solid Via Landing on a Non-Plated Layer

Stacked Microvias
Layer 1 – 2, 2 – 3, L8 - 7 & 7 - 6
0.012” pad & 0.006” laser drill

Layer 2 - 7 = Buried Vias
0.018” pad & 0.008” drill

Layer 1 - 8 = Through-hole
0.020” pad & 0.010” drill

Finish Thickness = 0.042” +/- 0.005”
Second Generation Microvia Geometries:
Solid Via Landing on a Non-Plated Layer

Microsection After Buried Via (FLAT-WRAP™) Cycled To Failure
# of HATS cycles passed = 0.008” – 2,604 & 0.010” – 3,278

SMV™ - L1-L2/L2-L3
0.004” & 0.005” vias
Passed 5,000 HATS cycle
**Second Generation Microvia Geometries:**

**Stacked MicroVia Landing on a Non-Plated Layer**

---

**Example 3:** Three layer stacked microvia (+3) terminating on a Cu foil layer. In this example Stacked vias are making a connection from layer 1 to layer 4 where layer 4 is the second layer of the primary sub lamination thereby terminating on a foil layer. Vias from layer 2 to 3 and 1 to 2 both require sequential lamination and as a result become plated layers adding additional thickness. In Addition, layers 2 and 4 are shown as plane layers however, they could just as easy be signal layers, the important point to note, is that copper thickness is dependant on specific stack-up requirements since build-up layers do require copper plating.
Second Generation Microvia Geometries:
Stacked MicroVia Landing on a Non-Plated Layer

Stacked MicroVia (SMV®)
L1-L2, L1-L3 & L1-L4
Finish Thickness = 0.062” +/- 0.007”
Material = High Temperature FR4
Second Generation Microvia Geometries
Solution for sub 0.5 mm pitch arrays

Microsection After Buried Via (FLAT-WRAP™) Cycled To Failure

# of HATS cycles passed = 0.25 mm – 1,337 & 0.3 mm – 1,716

20 Layer, 3+N+3, Stacked Microvia / Staggered Buried Via

PCB Thickness 2.46 mm +/- 10%

SMV® - L1-L2/L2-L3/L3-L4

# of HATS cycle passed
0.1 mm vias – 3,513
0.127 mm vias – 5,000
Chip Scale BGA Escape using Stacked Microvias

Section A-A: 4 layer stacked microvia structure*

*Only top 5 layers of the board are shown
Microvia Sub-lamination Interface Techniques
Advanced PCB Structures using Stacked Microvias

- Solid copper microvias can be vertically stacked to gain deeper penetration to internal layers (Design Flexibility)

- In general, laser direct imaging is recommended for proper registration in high density PCB applications

- Stacked microvias require sequential lamination for each additional layer

- The number of vertically stacked layers is limited by the number of lamination cycles that materials are exposed to. In general, most laminates should not be exposed to more than three thermal lamination cycles (4 – 5 Advanced)

- Stacked microvias start with a plating cycle to develop a solid copper filled via, followed by a pattern plate cycle to produce the circuit image. Therefore, the pattern plate thickness must be accounted for in the circuit design
Microvia stacked on Epoxy-filled Mechanical Via – NO!
Microvia Sub-Lamination Interface: Stacked On Sub-Via

- This approach requires via fill and wrap plating
- CTE issues can be a problem on thick boards

Not Recommended on all designs: Contact engineering
Microvia Sub-Lamination Interface: Offset Via

0.5 mm Pitch or >

Preferred Construction
Microvia Sub-Lamination Interface: Offset Via Stacked

0.4 mm Pitch or <

Preferred Construction
Microvia Sub-Lamination Interface: Sub-Lam Microvia

Preferred Construction with additional low cost Microvia to layer 4
Next Generation - SMV™ Technology
Next Generation - SMV™ Technology

We’re constantly working to enable new technologies to meet the needs of high-technology customer demands with small, feature-rich products (ex. mobile phones, PDA, cameras, and other such products).

- **NextGen - SMV™ Technology:**
  - Requires one to two lamination cycle (based on design constraint), reducing fabrication time
  - Eliminates plating cycle of inner layers
  - Improves inner layer characteristics, signal integrity and electrical characteristics
  - Reduces demand on plating and lamination, improving facility capacity utilization
  - Allows for thinner finished product
  - Initial customer builds have been encouraging with significant early interest
  - This is a Viasystems patented technology
NextGen Technology

Examples of three concepts that have been developed:

- **NextGen-SMV®** is a full build-up technology that is a single lamination parallel process (SLPP™) with conductive paste joints in the z-axis, provides Z-axis connectivity from, and to any layer.

- **HDI-Link™** is focused towards minimizing lamination cycles on designs such as 3+N+3 or 4+N+4 or ...where ‘N’ is a conventional buried via and 3+ or 4+ build-up cores utilize NextGen-SMV technology to make the connection in the Z-axis with conductive paste.

- **Sub-Link™** is solution for high aspect ratio PCB’s (> 40:1) where we build sub-section of a PCB and connect the subs with conductive paste in the Z-axis.
**NextGen-SMV™ Mass Terminated Microvia**

We continue to drive technology enhancements in the SMV™ arena:
- Requires one to two lamination cycle (based on design constraint), reducing fabrication time
- Eliminates plating cycle of inner layers
- Improves inner layer characteristics, signal integrity and electrical characteristics
- Reduces demand on plating and lamination, improving facility capacity utilization
- Allows for thinner finished product

---

**Step 1. Single sided core**

**Step 2. Single sided etched core**

**Step 3. Adhesive and single sided etched core**

**Step 4. Laser drilled micro vias**

**Step 5. Filled micro vias**

**Step 6. After single lamination**

- Laminate
- Protective film
- Metallic paste filler
- Copper foil
- Film adhesive

---

*TTM Technologies*
Single Lam vs. Sequential Build-up Process Comparison of 10L PCB

**Single Lamination Parallel Process**

1. **Material Issue**: Chemclean
2. **Resist Coat**
3. **Expose Image**
4. **DES**
5. **Oxide**
6. **Process 1**
7. **Process 2**
8. **Process 3**
9. **Process 4**
10. **Lamination**
11. **Tooling**
12. **Clean**
13. **Resist Coat**
14. **Expose Image**
15. **Final Process**
16. **Soldermask, Final Finish, Legend, Test**

**Industry Standard - Sequential Lamination**

1. **Material Issue**: Tooling
2. **Process A**
3. **Clean**
4. **Metallization**
5. **Resist Coat**
6. **Expose Image**
7. **Develop**
8. **Oxide**
9. **Layup and Lamination**
10. **Soldermask, Final Finish, Legend, Test**

**Next Steps**

- **Print Image**
- **Develop**
- **Process D**
- **Resist Strip**
- **Clean**
- **Metallization**
- **Resist Coat**
- **Process D**
- **Resist Strip**
- **Etch**
- **Clean**

**Repeat for**
- sub 3 to 6
- sub 2 to 8
- sub 4 to 7
- final 1 to 10
Copper vs. Conductive Paste

- Inner layers are plated vs. print and etch = contrasting thickness of copper
- Differing thermal conductivity; Copper (385 W/mK) vs. Paste (25 to 40 W/mK)
- Bulk Resistivity; Copper (1.7 micro ohm cm vs. 50 micro ohm cm)
NextGen capability
30 layer any layer via connectivity
**Guidelines for single shot lamination**  
**8 to 12 layer PCB**

<table>
<thead>
<tr>
<th></th>
<th>Standard</th>
<th>Advanced</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Lead Time</strong></td>
<td>7 days</td>
<td>5 days</td>
<td>3 days</td>
</tr>
<tr>
<td><strong>Layer Count</strong></td>
<td>up to 10</td>
<td>12 to 14</td>
<td>up to 18</td>
</tr>
<tr>
<td><strong>Dielectric Thickness</strong></td>
<td>0.081mm</td>
<td>0.081 &amp; 0.094mm</td>
<td>0.069 &amp; 0.107mm</td>
</tr>
<tr>
<td><strong>Via Diameter</strong></td>
<td>0.152mm</td>
<td>0.127 &amp; 0.152mm</td>
<td>0.1mm</td>
</tr>
<tr>
<td><strong>Pad Diameter</strong></td>
<td>0.279mm</td>
<td>0.25 &amp; 0.279mm</td>
<td>0.23mm</td>
</tr>
<tr>
<td><strong>Board Thickness</strong></td>
<td>1.0mm</td>
<td>1.2 &amp; 1.32mm</td>
<td>1.55 &amp; 2.0mm</td>
</tr>
<tr>
<td><strong>Impedance</strong></td>
<td>10 %</td>
<td>8 %</td>
<td>5 %</td>
</tr>
<tr>
<td><strong>Copper Weight</strong></td>
<td>18 µm</td>
<td>18 µm</td>
<td>12 to 18 µm</td>
</tr>
<tr>
<td><strong>Material Type</strong></td>
<td>High Temp FR4, Halogen Free</td>
<td>Low Loss Epoxy, BT, Halogen Free</td>
<td>High Speed</td>
</tr>
</tbody>
</table>
DDi HDI-Link™, Sub-to-core attach

Conventional 4 Lam 10 Layer 3+N+3 Build PCB

NextGen 2 Lam 10 Layer HDI-Link™ Build PCB
Example of HDI-Link™
20 layer PCB with 3+N+3 construction

Sub-to-Core Attach
Example of HDI-Link™ 14 layer PCB
3+N+3 (buried via = solid copper plate)
# 2 lamination cycle PCB build
## Conventional buried via (N) + NextGen layers

<table>
<thead>
<tr>
<th></th>
<th>Standard</th>
<th>Advanced</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Lead Time</strong></td>
<td>10 days</td>
<td>7 days</td>
<td>5 days</td>
</tr>
<tr>
<td><strong>Layer Count</strong></td>
<td>3+N+3</td>
<td>4+N+4</td>
<td>5+N+5</td>
</tr>
<tr>
<td><strong>Dielectric Thickness</strong></td>
<td>0.081</td>
<td>0.081 &amp; 0.094mm</td>
<td>0.069 &amp; 0.107mm</td>
</tr>
<tr>
<td><strong>Via Diameter</strong></td>
<td>0.152mm</td>
<td>0.127 &amp; 0.152mm</td>
<td>0.1mm</td>
</tr>
<tr>
<td><strong>Pad Diameter</strong></td>
<td>0.279mm</td>
<td>0.25 &amp; 0.279mm</td>
<td>0.23mm</td>
</tr>
<tr>
<td><strong>Board Thickness</strong></td>
<td>1.5mm</td>
<td>3.0mm</td>
<td>5.0mm</td>
</tr>
<tr>
<td><strong>Impedance</strong></td>
<td>10 %</td>
<td>8 %</td>
<td>5 %</td>
</tr>
<tr>
<td><strong>Copper Weight</strong></td>
<td>18 μm</td>
<td>18 μm</td>
<td>12 &amp; 18 μm</td>
</tr>
<tr>
<td><strong>Material Type</strong></td>
<td>High Temp FR4, Halogen Free</td>
<td>Low Loss Epoxy, BT, Halogen Free</td>
<td>High Speed</td>
</tr>
</tbody>
</table>
DDi Sub-Link™, Sub-to-Sub Attach

Conventional High Aspect Ratio PCB
30 + Layers Build PCB

DDi Sub-Link™ High Aspect Ratio PCB
30 + Layers
DDi Sub-Link™ - Solution for high aspect ratio PCBs
Example of 32 layer Load Board; 11+10+11

Sub-to-Sub Attach

- Sub-Link™ (sub-to-sub attach)
  - Three subs (about 0.060” thick) were used as proof-of-concept
  - Developed a new concept for sub connectivity with conductive paste
  - Solid copper vias in subs with 0.006” mechanical drilled holes
  - PCB pass IPC standard electrical test requirement
DDi Sub-Link, Sub-to-Sub Attach

Sub-Link - Sub-to-Sub Attach
Solution for High Aspect Ratio PCB
## NextGen Sub-Link™ Design Guidelines

<table>
<thead>
<tr>
<th>DDi Sub-Link™ BOARD CHARACTERISTICS</th>
<th>Standard</th>
<th>Advanced</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Lead Time</strong></td>
<td>15 days</td>
<td>12 days</td>
<td>7 days</td>
</tr>
<tr>
<td><strong>Layer Count</strong></td>
<td>3 Subs</td>
<td>4 Subs</td>
<td>5 Subs</td>
</tr>
<tr>
<td><strong>Dielectric Thickness</strong></td>
<td>Standard core and prepreg thickness</td>
<td>Standard core and prepreg thickness</td>
<td>Standard core and prepreg thickness</td>
</tr>
<tr>
<td><strong>Via Diameter</strong></td>
<td>0.152mm</td>
<td>0.127mm</td>
<td>0.1mm</td>
</tr>
<tr>
<td><strong>Pad Diameter</strong></td>
<td>0.279mm</td>
<td>0.25mm</td>
<td>0.23mm</td>
</tr>
<tr>
<td><strong>Board Thickness</strong></td>
<td>4.6mm</td>
<td>6.0mm</td>
<td>7.62mm</td>
</tr>
<tr>
<td><strong>Impedance</strong></td>
<td>10 %</td>
<td>8 %</td>
<td>5 %</td>
</tr>
<tr>
<td><strong>Aspect Ratio</strong></td>
<td>30:1</td>
<td>40:1</td>
<td>50:1</td>
</tr>
<tr>
<td><strong>Material Type</strong></td>
<td>High Temp FR4, Halogen Free</td>
<td>Low Loss Epoxy, BT, Halogen Free</td>
<td>High Speed</td>
</tr>
</tbody>
</table>
NextGen Extension
Enable HDI in Rigid-Flex PCBs

Rigid-Flex PCB with DDi NextGen-SMV®
PPSL™ - Parallel Process Single lamination (all paste connectivity in the z-axis)
Microvia Sub-lamination Interface Techniques
Microvia: Sub-Lamination Interface

Basic design rules for Microvia build-up layers

- Build-up dielectric layers must be balanced on either side of the sub-lamination

- Build-up dielectric layers are generally 0.0025” (64µm) to 0.003” (75µm) thick

- The recommended total number of lamination cycles that any one part of the structure should experience is 3 and 4 – 5 for advanced structures

- Microvias stacked on buried mechanical vias should be avoided due to wrap plating requirements and excessive stress on thicker substrates

- Solid copper mechanically drilled vias can be used on thin sub-lamination cores in place of wrap plating
Microvia stacked on Epoxy-filled Mechanical Via – NO!
Microvia Sub-Lamination Interface: Stacked On Sub-Via

- This approach requires via fill and wrap plating
- CTE issues can be a problem on thick boards

Not Recommended on all designs: Contact engineering
Microvia Sub-Lamination Interface: Offset Via

0.5 mm Pitch or >

Preferred Construction
Microvia Sub-Lamination Interface: Offset Via Stacked

0.4 mm Pitch or <

Preferred Construction
Microvia Sub-Lamination Interface: Sub-Lam Microvia

Preferred Construction with additional low cost Microvia to layer 4
Via-in-Pad, Wrap Plate, & FLAT-WRAP™
Standard Construction vs. Via-In-Pad circuit Construction

By using either conductive or non-conductive fillers and over plating with copper, through hole vias can be placed in component pads with no impact on the soldering process.
### Table 3-3 Surface and Hole Copper Plating Minimum Requirements for Buried Vias ≥ 2 Layers, Through-Holes and Blind Vias

<table>
<thead>
<tr>
<th></th>
<th>Class 1</th>
<th>Class 2</th>
<th>Class 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper - average</td>
<td>20 μm [787 μin]</td>
<td>20 μm [787 μin]</td>
<td>25 μm [984 μin]</td>
</tr>
<tr>
<td>Thin areas</td>
<td>18 μm [709 μin]</td>
<td>18 μm [709 μin]</td>
<td>20 μm [787 μin]</td>
</tr>
<tr>
<td>Wrap</td>
<td>AABUS</td>
<td>5 μm [197 μin]</td>
<td>12 μm [472 μin]</td>
</tr>
</tbody>
</table>

**Note 1.** Does not apply to microvias. Microvias are vias that are ≤0.15 mm [0.006 in] in diameter and formed either through laser or mechanical drilling, wet/dry etching, photo imaging or conductive ink formation followed by a plating operation. Blind vias with aspect ratios less than 1:1 shall be treated as microvias for plating thickness requirements. See Table 3-4.

**Note 2.** Copper plating (1.3.4.2) thickness shall be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

**Note 3.** Wrap copper plating for filled PTHs and vias shall be in accordance with 3.6.2.11.1.

**Note 4.** See 3.6.2.11.

### Table 3-4 Surface and Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried)

<table>
<thead>
<tr>
<th></th>
<th>Class 1</th>
<th>Class 2</th>
<th>Class 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper - average</td>
<td>12 μm [472 μin]</td>
<td>12 μm [472 μin]</td>
<td>12 μm [472 μin]</td>
</tr>
<tr>
<td>Thin areas</td>
<td>10 μm [394 μin]</td>
<td>10 μm [394 μin]</td>
<td>10 μm [394 μin]</td>
</tr>
<tr>
<td>Wrap</td>
<td>AABUS</td>
<td>5 μm [197 μin]</td>
<td>6 μm [236 μin]</td>
</tr>
</tbody>
</table>

**Note 1.** Microvias are vias that are ≤ 0.15 mm [0.006 in] in diameter and formed either through laser or mechanical drilling, wet/dry etching, photo imaging or conductive ink formation followed by a plating operation. The values given for blind and buried microvias are not applicable for stacked microvias. As of the publication of this specification, there is little known about this structure and the reliability results are not consistent with buried and blind microvias. Stacked microvias may also require different inspection criteria.

**Note 2.** Copper plating (1.3.4.2) thickness shall be continuous and wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

**Note 3.** Wrap copper plating for filled microvias shall be in accordance with 3.6.2.11.1.

**Note 4.** See 3.6.2.11.
### IPC 6012C Specification For Wrap Plating Thickness

#### Table 3-5 Surface and Hole Copper Plating Minimum Requirements for Buried Via Cores (2 Layers)

<table>
<thead>
<tr>
<th></th>
<th>Class 1</th>
<th>Class 2</th>
<th>Class 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper - average(^1,3)</td>
<td>13 µm [512 µin]</td>
<td>15 µm [592 µin]</td>
<td>15 µm [592 µin]</td>
</tr>
<tr>
<td>Thin areas(^3)</td>
<td>11 µm [433 µin]</td>
<td>13 µm [512 µin]</td>
<td>13 µm [512 µin]</td>
</tr>
<tr>
<td>Wrap(^2)</td>
<td>AABUS</td>
<td>5 µm [197 µin]</td>
<td>7 µm [276 µin]</td>
</tr>
</tbody>
</table>

**Note 1.** Copper plating (1.3.4.2) thickness shall be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

**Note 2.** Wrap copper plating for filled buried via cores shall be in accordance with 3.6.2.11.1.

**Note 3.** See 3.6.2.11.

---

**Figure 3-17** Wrap Copper in Type 4 Printed Board (Acceptable)

**Figure 3-18** Wrap Copper Removed by Excessive Sanding/Planarization (Not Acceptable)
Filled Via With Wrap Plating

Pattern plate copper
Electroless copper
Panel plate copper
3/8 oz Copper foil
Electroless copper

Continuous electrolytic copper plating from hole barrel to pad surface "Wrap"

Conductive or Non-conductive filler
Filled Via With Wrap Plating (VIPPO)

- Pattern plate
- Wrap plate
- Cu Foil

Conductive Via fill

Non-conductive Via fill
**FLAT-WRAP™** Technology allows wrap plating and multiple wrap plating cycles with no copper buildup
What Happens When More Than One Wrap Plating Cycle Is Required?

Conventional Wrap Plating
(3x wrap on a common layer)

- 1st Wrap Plate Required
- Via Fill
- Cu Pattern Plate
- Cu Panel Plate
- Cu Foil
- Total surface copper after 3x wrap

FLAT-WRAP™
(3x wrap on a common layer)

- 2nd Wrap Plate Required
- Via Fill
- Cu Foil + 3x Wrap plate cycles
- Total surface copper after 3x wrap (Equal to starting base foil thickness)

- 3rd Wrap Plate Required
- Via Fill
- Cu Pattern Plate
- Cu Foil
- Cu Foil

TTM Technologies


**FLAT-WRAP™ Technology**

Current standard for
IPC 6012B Class 3, 3 x wrap

DDi’s **FLAT-WRAP™ Technology**
IPC 6012B Class 3, 3x wrap

- Industry specification (IPC 6012C) requires wrap-around plating for filled blind and buried via technology

- Current industry practices produce excessive plated copper on the required layer and limits the capability for surface feature packaging density (LWS dimensions)

- **FLAT-WRAP®** technology reduces surface copper thickness on multiple lamination product and enables finer geometries and facilitates improved design capabilities
### Wrap Plating Design Guideline Comparison

#### Conventional Wrap Plate Design Guidelines

<table>
<thead>
<tr>
<th>Design Rule</th>
<th>IPC 6012 Class 2 - assume a starting copper foil of 3/8 oz</th>
<th>IPC 6012 Class 3 - assume a starting copper foil of 3/8 oz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>No Wrap</td>
<td>1 X Wrap</td>
</tr>
<tr>
<td>Preferred</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.003&quot; Line</td>
<td>0.005&quot; Line</td>
</tr>
<tr>
<td></td>
<td>0.0035&quot; Space</td>
<td>0.005&quot; Space</td>
</tr>
<tr>
<td>Advanced capability = reduced yield (call engineering prior to quote)</td>
<td>0.003&quot; Line</td>
<td>0.004&quot; Line</td>
</tr>
<tr>
<td></td>
<td>0.003&quot; Space</td>
<td>0.005&quot; Space</td>
</tr>
</tbody>
</table>

Note: Due to the overhang (caused by undercut during etch) all Gold body jobs or designs that utilize Gold as an etch resist and require wrap plating to meet IPC 6012, Class 2 or 3 specification, will need engineering approval prior to quote …… no exceptions

### FLAT-WRAP™ Technology Design Guidelines

<table>
<thead>
<tr>
<th>Design Rule</th>
<th>IPC 6012 Class 2 - Starting copper weight 3/8 oz</th>
<th>IPC 6012 Class 3 - Starting copper weight 1/2 oz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>No Wrap</td>
<td>1 X Wrap</td>
</tr>
<tr>
<td>Preferred</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.003&quot; Line</td>
<td>0.003&quot; Line</td>
</tr>
<tr>
<td></td>
<td>0.0035&quot; Space</td>
<td>0.0035&quot; Space</td>
</tr>
<tr>
<td>Advanced capability = reduced yield (call engineering prior to quote)</td>
<td>0.003&quot; Line</td>
<td>0.003&quot; Line</td>
</tr>
<tr>
<td></td>
<td>0.003&quot; Space</td>
<td>0.003&quot; Space</td>
</tr>
</tbody>
</table>

Note: Gold body jobs or designs that utilize Gold as an etch resist and require wrap plating to meet IPC 6012, Class 2 or 3 specification, will not need engineering approval if PCB's are fabricated with this new technology
# FLAT-WRAP™ - Reliability Test Matrix

<table>
<thead>
<tr>
<th>Description of Tests</th>
<th>Remarks</th>
<th>Test Status</th>
<th>Test Results</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Manufacturability Tests</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>As received - Microsection PTH Quality</td>
<td>Plated Barrel Copper Thickness 260 (500)</td>
<td>Completed</td>
<td>Passed</td>
</tr>
<tr>
<td><strong>Pb-Free Assy Process Compatibility</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Solder Float Test - Microsection PTH Quality</td>
<td>Temperature Deg C (Deg F) 260 (500)</td>
<td>Completed</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Pb Free Reflow Assembly Simulation</strong></td>
<td>Temperature Deg C (Deg F) 260 (500)</td>
<td>Completed</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Reliability Tests</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IST - Interconnect Stress Test</td>
<td>IST Pre-conditioning cycles at 260 C 4X</td>
<td>Completed</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HATS - Highly Accelerated Thermal Shock</td>
<td>Pb Free Assembly Profile Pre-conditioning, peak temp 260 C 4X</td>
<td>Completed</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Remarks**
- Microsection analysis performed by DDi
- BGA coupons - DDi
- Microtek Labs to process BGA coupons through Pb Free profile through IR Reflow oven and DDi to do microsection analysis
- 3 coupons / preconditioning (Total of 18 coupons). Dual sense test performed by DDI VA. Two different test conditions with San-Ei & CB100 via fill materials
- IST testing to be performed by PWB Corp, Dual Sense to 1000 cycles
- 12 coupons tested. Test performed by Microtek Labs. Two different test conditions with San-Ei & CB100 via fill materials

**Test Results**
- Passed
- Completed
C²eT
Controlled Copper Etch Technology
Precision Features For RF and Microwave Applications
Why Use Foil Only Features?

- Precession etching for microwave antenna
- Integrated Microwave Circuits
- Filters and other precision etched components

Automotive Radar
Why Use Foil Only Features?

- RF and microwave circuits generally require printed components such as antenna, filters, couplers, resonators and precision taps.
- As frequencies increase printed component size decreases with a demand for improved conductor resolution i.e. precise trace and space.
- Current designs are demanding finished trace and space tolerance to be $+/- 0.0005”$ to $0.0007”$ (predicated on customers demand for performance).
- Pattern plating on surface layers reduced conductor resolution.
- Via-In-Pad required in many designs introduces wrap plating, increasing the background copper that must be etched, further reducing resolution.
- Producing Foil Only etched features eliminates the plating and wrap plating in feature regions improving resolution.
Applications In RF & Microwave Circuits

Pattern plating process for via plating and non-critical circuit formation

Filter image etched into Outer layer foil, no plating

Mask overlap region; typically 6 mils
Sample stack-up of RF & Microwave job

Layer 1: Laminate Core
Layer 2: Prepreg
Layer 3: Laminate Core
Layer 4: Mixed Signal Layer

Mechanical drill standard pattern plating
RF Signal Layer
Mixed Signal Layer
Laser drill standard pattern plating

1/2 oz + Plt
1/2 oz
370 HR 2X 106
1/2 oz
370HR 0.008”
Rogers 6002 0.010”
Example of PCB Outer Layer

RF Outer Layer With Printed Filters

- Foil region consists of only foil and Cu flash plate
- Pattern plate region, standard copper thickness
- Photo tools are required for:
  - Foil only print and etch
  - Pattern plate tools with foil only isolation
  - Foil only photo tool to protect Foil Only region in final etch
Foil Only Features On Surface Plated Layers

Standard copper pattern plate

Plated region
Transition region
Foil region

Trace cross-section A-A

Transition region

Foil only region

Length = 0.00137 inch COPPER ONLY
Length = 0.00069 inch COPPER ONLY
Length = 0.0008 inch OVERALL
Length = 0.00153 inch OVERALL
Advanced Thermal Management Techniques
Thermal Conduction In PCBs

Heat Flow

- Die
- IC Package
- Lead / Balls
- Printed Circuit
- Enclosure / Rack
- Environment

Thermal resistance at each level of an electronic system will impact conduction...

...Heat generated must go somewhere!

Relative surface area
Factors Increasing Thermal Density

- Dramatic increase in Semiconductor power
- Rapid reduction in component size

Power dissipation 3 watts
Power density 1.08 watts/cm

Density increase

Power dissipation 3 watts
Power density 3.7 watts/cm
Thermal Conductivity

Thermal conductivities of common PCB materials

- Copper: 0.0 W/m · K
- Silver: 0.3 W/m · K
- Gold: 1.0 W/m · K
- Nickel: 0.64 W/m · K
- Aluminum: 1.0 W/m · K
- Solder: 0.64 W/m · K
- Stablcor: 10 W/m · K
- FR-4: 10 W/m · K
- Ceramic: 0.64 W/m · K
- CB-100: 0.64 W/m · K
- TC350: 0.64 W/m · K
- RO4350: 0.64 W/m · K
Common dielectric materials have relatively low thermal conductivities where as electrical conductors have relatively high conductivities…

Increased thermal conductivity is achieved with conductors
Thermal Via Applications

Thermal pad for conducting heat from the component to internal planes or external heat sink on the back of the board.

Issues: Through holes will wick solder away from the component connection and deposit on the back side of the board!

Via-In-Pad Construction

Plated through hole provide a thermal shunt resistance bypassing the dielectric layer.

Assembly issues have been eliminated!
Thermal Resistance: Parallel Thermal Vias

Note: Thermal vias’ s placed in a 1.0 cm (0.0394) square
Common thermal via constructions:

- Standard
- Conductive Filled
- Thicker Copper

Copper = 380 W/m K
Conductive filler = 3.5 to 6.7 W/m K
Thermal Resistance vs Via Technologies

Thermal via length in mm

Thermal resistance K/W

Drill diameter
- 0.001" (0.025 mm) copper plating
- 0.001" (0.025 mm) copper plating conductive filler 6.7 W/mK
- 0.002" (0.05 mm) copper plating

All plated through holes 0.012" (0.3 mm) dia.

Thermal via length in mm
Solid Copper Via

- 0.010” Diameter

- Process to provide solid copper fill at accelerated plating rates
- 10:1 aspect ratios are currently achievable
- Applications include:
  - Low resistance via’s allowing high current or reduced diameter
  - Thermal via’s with high conductivity
  - Potential replacement for wrap plating
Thermal Resistance Parallel Vias

Note: Thermal vias placed in a 1.0 cm (0.0394) square.
Long term PCB Technology Roadmap
<table>
<thead>
<tr>
<th>Line / Space</th>
<th>Internal</th>
<th>0.0025&quot; / 0.003&quot;</th>
<th>0.0025&quot; to 0.002&quot; / 0.003&quot; to 0.0025&quot;</th>
<th>0.002&quot; / 0.0020&quot;</th>
<th>0.0015&quot; to 0.002&quot; / 0.0015&quot; to 0.0020&quot;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>External</td>
<td>0.003&quot; / 0.0035&quot;</td>
<td>0.003&quot; to 0.0025&quot; / 0.003&quot; to 0.0025&quot;</td>
<td>0.002&quot; / 0.002&quot;</td>
<td>0.0015&quot; / 0.002&quot;</td>
</tr>
<tr>
<td>Plated Layer Etch Tolerance</td>
<td>+/- 0.001&quot; to +/- 0.0005&quot;</td>
<td>+/- 0.00075&quot; to 0.0005&quot;</td>
<td>+/- 0.0005&quot;</td>
<td>+/- 0.0003&quot;</td>
<td>+/- 0.0003&quot;</td>
</tr>
<tr>
<td>Drilled Via</td>
<td>Drill Size</td>
<td>0.010&quot; / 0.008&quot; / 0.006&quot;</td>
<td>0.010&quot; / 0.008&quot; / 0.006&quot;</td>
<td>0.008&quot; / 0.006&quot;</td>
<td>0.006&quot; / 0.004&quot;</td>
</tr>
<tr>
<td></td>
<td>Pad Size</td>
<td>0.020&quot; / 0.018&quot; / 0.016&quot;</td>
<td>0.018&quot; / 0.016&quot; / 0.014&quot;</td>
<td>0.014&quot; / 0.012&quot;</td>
<td>0.012&quot; / 0.010&quot;</td>
</tr>
<tr>
<td></td>
<td>Hole to Cu</td>
<td>0.008&quot; to 0.006&quot;</td>
<td>0.007&quot; to 0.006&quot;</td>
<td>0.006&quot; to 0.005&quot;</td>
<td>0.005&quot; to 0.004&quot;</td>
</tr>
<tr>
<td>Via Fill (Via-In-Pad)</td>
<td>10:1 to 12:1 (ATE 31:1)</td>
<td>12:1 to 16:1 (ATE 31:1)</td>
<td>16:1 to 20:1 (ATE 40:1)</td>
<td>20:1 to 24:1 (ATE 40:1)</td>
<td>24:1 to 30:1 (ATE 50:1)</td>
</tr>
<tr>
<td>BGA Pitch</td>
<td>0.65mm / 0.5mm / 0.4mm</td>
<td>0.5mm / 0.4mm</td>
<td>0.5mm / 0.4mm</td>
<td>0.4mm / 0.3mm</td>
<td>0.4mm / 0.3mm</td>
</tr>
<tr>
<td>Micro Via</td>
<td>Via Size</td>
<td>0.006&quot; / 0.005&quot; / 0.004&quot;</td>
<td>0.005&quot; / 0.004&quot;</td>
<td>0.005&quot; / 0.004&quot;</td>
<td>0.004&quot; / 0.003&quot;</td>
</tr>
<tr>
<td></td>
<td>Pad Size</td>
<td>0.012&quot; / 0.010&quot; / 0.009&quot;</td>
<td>0.010&quot; / 0.009&quot; / 0.008&quot;</td>
<td>0.009&quot; / 0.008&quot;</td>
<td>0.008&quot; / 0.006&quot;</td>
</tr>
<tr>
<td>Micro Via Aspect Ratio</td>
<td>0.6:1 to 1:1</td>
<td>0.8:1 to 1.2:1</td>
<td>1:1 to 1.25:1</td>
<td>1.25:1</td>
<td>1.25:1</td>
</tr>
<tr>
<td>CSP Pitch</td>
<td>0.3mm / 0.25mm</td>
<td>0.3mm / 0.25mm</td>
<td>0.25mm / 0.2mm</td>
<td>0.2mm / 0.15mm</td>
<td>0.15mm / 0.10mm</td>
</tr>
<tr>
<td>Micro Via</td>
<td>Via Size</td>
<td>0.004&quot;</td>
<td>0.004&quot; / 0.003&quot; to 0.002&quot;</td>
<td>0.004&quot; / 0.003&quot; to 0.002&quot;</td>
<td>0.002&quot; via or fan out from standard 0.004&quot; microvia structures</td>
</tr>
<tr>
<td></td>
<td>Pad Size</td>
<td>0.008&quot; / 0.0068&quot;</td>
<td>0.008&quot; / 0.006&quot;</td>
<td>0.006&quot; / 0.005&quot;</td>
<td>0.004&quot;</td>
</tr>
<tr>
<td>Line &amp; Space - SMV with perimeter rout using std design</td>
<td>Perimeter rout only w ith 0.003&quot; / 0.0035&quot; design rule</td>
<td>Perimeter rout only w ith 0.0025&quot;/0.003&quot; design rule</td>
<td>Perimeter rout only w ith 0.002&quot;/0.0025&quot; design rule</td>
<td>Perimeter rout only w ith 0.002&quot;/0.002&quot; design rule</td>
<td>Perimeter rout only w ith 0.0015&quot; / 0.002&quot; design rule</td>
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</tbody>
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<thead>
<tr>
<th></th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
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</thead>
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<tr>
<td></td>
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<tr>
<td>Micro Via Aspect Ratio</td>
<td>0.6:1 to 1:1</td>
<td>0.8:1 to 1.2:1</td>
<td>1:1 to 1.25:1</td>
<td>1:1 to 1.25:1</td>
<td>1:1 to 1.25:1</td>
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<tr>
<td>SMV &amp; High Aspect Ratio Seed Metallization &amp; Electroplating</td>
<td>4+N+4, evaluate PPR vs. DC</td>
<td>One step copper fill + pattern plate</td>
<td>High speed plating system</td>
<td>Plating distribution +/- 10%</td>
<td>High Speed High Throw Plating System &amp; Chemistry</td>
</tr>
<tr>
<td></td>
<td>One step copper fill + pattern plate</td>
<td>Vertical vs. Horizontal</td>
<td>Low temp vapor deposition of copper</td>
<td>Fully additive process</td>
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</tr>
<tr>
<td>SMV NextGen</td>
<td>Reliability testing and production readiness</td>
<td>Phase II, expand capabilities</td>
<td>Integrate to Occam (explore)</td>
<td>Leverage modular concept to next level stacking application</td>
<td></td>
</tr>
<tr>
<td>Expand R-Flex Capability</td>
<td>Instal SMV process in OH</td>
<td>Rigid Flex capability in AH (should we explore the)</td>
<td>CSP on R-Flex BC &amp; BR in R-Flex PCB</td>
<td>Embedded Components</td>
<td>Embedded Components</td>
</tr>
<tr>
<td></td>
<td>Pb Free &amp; Halogen Free, low Tg filled, High Perfromance filled, Z-axis Interconnect w ith conductive paste</td>
<td>Film based materials, High Perfromance Filled, FEP and bonding film</td>
<td>Advanced RF application</td>
<td>Film based, 0.001&quot; to 0.002&quot;</td>
<td>Film based, 0.001&quot; to 0.002&quot;</td>
</tr>
<tr>
<td>Materials</td>
<td></td>
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<tr>
<td>Surface Finishes</td>
<td>ENePig (Universal Finish), Pb Free HASL, depends on market demand</td>
<td>Ormecon (Ag finish using nano technolgy)</td>
<td>Electroless Gold (Neutral), depends on market demand</td>
<td>Direct Immersion Gold (DIG), depends on market demand</td>
<td>Nano technology surface finishes</td>
</tr>
<tr>
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<tr>
<td>Equipment / Process</td>
<td>LDI Solder Mask &amp; Maskless Lithography, XACT, Pinnless Lamination, Vision Drill 180K+RPM</td>
<td>Maskless or Ink Jet Solder Mask, Vision Drill &amp; Rout with variable RPM</td>
<td>Ink Jet Liquid Photo Resist, Next Generation Laser Drill</td>
<td>Quick Lamination Press</td>
<td>High speed laser structuring systems or w ater jet technology</td>
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<tr>
<td>Embedded Technology - Passives &amp; Actives</td>
<td>EPT (BC = ultra thin filled substrate (&lt;0.001&quot;) / BR = Ohmega &amp; TICER)</td>
<td>Embedded Active Technology - Active devices in PCB (IC, capacitors, resistors, etc.)</td>
<td></td>
<td>Ink Jet Technology for BR</td>
<td>High Dk heavily filled materials</td>
</tr>
<tr>
<td>Thermal Management</td>
<td>Copper Core &amp; Stablcor</td>
<td>Copper Core &amp; Stablcor</td>
<td>Advanced materials with nano technology</td>
<td></td>
<td>Light weight thermally conductive and not electrically conductive</td>
</tr>
<tr>
<td>Future Technologies</td>
<td>Emb Active Tech, Embedded Circuit w / transfer technology and laser trench process, Photovoltaics, Optoelectronics, MEMS, Printable Electronics, and other industry demand</td>
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</table>

5 Year Technology Roadmap

<table>
<thead>
<tr>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
</tr>
</thead>
</table>

TTM Technologies
Viasystems Interconnect Technology

SMV®
DpMV™
DpSMV™
DpBV™
ThermalVia™

FLAT-WRAP™
NextGen-SMV®
HDI-Link™
Sub-Link™
Summary

Today’s Challenges are met by Enabling PCB Technologies...

• Start designs by defining the technology limiting packages
• Define the minimum technology set for the PCB design
• Look for a power delivery solution
• Review the design interactions with the technologies selected
• Make sure the technology level is compatible with your PCB supply chain
• Rethink design strategies before “bending” the rules

...Sometimes a little more time spent on a design can dramatically reduce cost
Thank you!

For further information, please contact:

Gil White, Site Sales Director, AH; gil.white@ttm.com; 714-815-5946
Julie Ellis, FAE; julie.ellis@ttm.com; mobile 714-473-1867
Marty Grasso, GAM; marty.grasso@ttm.com; mobile 714-813-8254
Ryan Joly, GAM; ryan.joly@ttm.com; mobile 714-323-3213